AMENDMENTS TO THE DRAWINGS

The attached sheet of drawing includes changes to Fig. 25. Fig. 25 is labeled PRIOR ART as directed by the Examiner.

Attachment: Replacement sheet

REMARKS

In response to the Office Action dated May 4, 2006, claims 17-20 are added. Claims 1-20 are now active in this application. No new matter has been added.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 102 AND § 103

I. Claims 1, 2, 4, 6, 7, 9, 11, 12, 14 and 16 are rejected under 35 U.S.C. § 102(a) as being anticipated by Fig. 25 and page 1 line 10 to page 5, line 9 of the specification (Applicant's Admitted Prior Art, hereinafter AAPA).

The rejections are respectfully traversed.

The Examiner has indicated that claim 1 lacks novelty, by referring to the description from page 4, line 18 to page 5, line 5 as explaining that:

> the source bus lines in the group 196 of Figure 25 have a capacitance of 20pF formed on them.

It seems, however, that the Examiner misunderstands the description. The description "the capacitance for each one of the second group 196 of lines is 20 pF (from page 4, line 25 to page 5, line 1)," to which the Examiner refers, does **NOT** mean that a capacitance of 20 pF is "added (i.e., ***formed*** intentionally)" to the second group 196 of lines, but means that the capacitance is 20 pF under the condition where no special capacitance is added to the second group 196 of lines. The capacitance of 20 pF is ***naturally*** (inevitably) generated at, for example, the intersection of a gate bus line 188 and a source bus line 189.

Each of independent claims 1, 6, 7 and 12 requires the positive act that a capacitance be "***formed***" on the recited line, which is clearly different from the capacitance that such line

inherently has as a natural property. In other words, "the capacitance of 20 pF", described as an example in AAPA, is essentially different from "the first capacitance" (formed thereon) which is a feature of the present invention.

Thus, it is clear that AAPA does not teach or suggest a "first capacitance formed" on at least one first bus line, which is recited in each of independent claims 1, 6, 7 and 12. Consequently, independent claims 1, 6, 7 and 12 are patentable over AAPA. Therefore, the allowance of independent claims 1, 6, 7 and 12, as well as of dependent claims 2, 4, 9, 11, 14 and 16, is respectfully solicited.

II. Claims 3, 5, 8, 10, 13 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Kurashima et al. (USPN 6,954,184).

However, as independent claims 1, 7 and 12 are patentable over AAPA, claims 3 and 5 depending from independent claim 1, claims 8 and 10 depending from independent claim 7, and claims 13 and 15 depending from independent claim 12, are patentable over AAPA also, even when considered in view of Kurashima et al. Consequently, the allowance of claims 3, 5, 8, 10, 13 and 15 is respectfully solicited also.

NEW CLAIMS

As noted above, the Examiner referred to the description from page 4, line 18 to page 5, line 5 as explaining that the source bus lines in the group 196 of Fig. 25 (each) have a capacitance of 20pF formed on them. Referring to the described example, the main panel 182 is presumed to have a capacitance of 20 pF and the sub-pane 183 is presumed of have a capacitance

of 10 pF. With these (naturally generated) capacitance, each bus line of the group 195 has a capacitance of 30 pF (20 pF + 10 pF) while each bus line of the group 196 only has a capacitance of 20 pF. The problem with such difference in (natural) capacitance of each bus line of group 195 from that of each bus line of group 196 is described from page 5, line 2 through line 9. That is:

> Upon producing a display on the main panel 182, the difference in capacitance renders differences in source signal delays distinct between the boundary between the first and second groups 195, 196, causing block split and other display defects. "Block split" is an irregular display which occurs in a certain block of a display panel, and caused by difference in delay among signals on lines arranged to form a matrix in the display panel.

More specifically, signal delay on each bus line of group 195 (having a greater capacitance that each bus line of group 196) is longer than on each bus line of group 196. This delay difference causes "block split" as well as other display defects.

To address such problem, the present application discloses (intentionally) ***forming*** a first capacitance on at least one of the first bus lines (at least one of the source bus lines 4 of Fig. 1 of the present application), and an amount of the first capacitance is such that there is substantially ***no difference in signal delay*** on the at least one source bus line 4 as compared with each source bus line 5.

New claims 17-20 are added and depend respectively from independent claims 1, 6, 7 and 12. New dependent claim 17 recites:

> ...wherein
> an amount of the first capacitance is such that there is substantially no difference in signal delay on each first bus line of the active matrix substrate that is connected to a first bus line on the other active matrix substrate and signal delay on the at least one first bus line with a first capacitance.

New dependent claims 18-20 have similar recitations.

As described above, AAPA (Fig. 25) clearly does not disclose (intentionally) ***forming*** a first capacitance on at least one of the first bus lines, let alone that the (intentionally) formed first capacitance is in an amount such that there is substantially no difference in signal delay on each source bus line (of group 195) of the active matrix substrate (184 of main panel 182) that is connected to a first bus line on the other active matrix substrate (186 of sub-panel 183) and signal delay on the at least one first bus line with a first capacitance (any one of the source bus lines of group 196).

In view of the above, dependent claims 17-20 are patentable over AAPA, for reasons in addition to the reasons as to why independent claims 1, 6, 7 and 12 are patentable over AAPA. Therefore, the allowance of new claims 17-20 is respectfully solicited.

CONCLUSION

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Edward J. Wise (Reg. No. 34,523) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

CG/EJW/vd

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

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Attachment: Replacement Drawing (Fig. 25)

CG/EJW/vd